Sample and Hold (S/H)

Sample and Hold (S/H)

- "Sample and Hold" is often referred to as "Track and hold"(T/H)
  - Identical in both function & circuit implementation in most cases
  - Only distinction: How they are used in the system
    - S/H: Samples the input for a short time and stays in the hold mode for the remainder of the cycle
    - T/H: Spends most of the time tracking the input and is switched into the hold mode for only brief interval
  - In general: These two terms are used interchangeably

- Necessary components in many data-acquisition systems such as A/D converters

Performance Parameters of S/Hs

- Sampling pedestal or a hold step
  - Error that occurs each time a sample and hold goes from sample mode to hold mode
  - During this change in operation, there is always a small error in the voltage being held that makes it different from the input voltage at the time of sampling.
  - Obviously, this error should be as small as possible. Perhaps more importantly, this error should be signal independent; otherwise it can introduce nonlinear distortion.
- How isolated the sampled signal is from the input signal during hold mode
  - Ideally, the output voltage will no longer be affected by changes in the input voltage
  - In reality, there is always some signal feedthrough, usually through parasitic capacitive coupling from the input to the output. In well-designed sample and holds, this signal feedthrough can be greatly minimized.

Performance Parameters of S/Hs (Cont.)

- The speed at which a sample and hold can track an input signal, when in sample mode.
  - In this mode, a sample and hold will have both small-signal and large-signal limitations due to its -3dB bandwidth and finite slew rate, respectively.
  - Both the -3dB bandwidth and slew rate should be maximized for high-speed operation.

- Droop rate in hold mode
  - Somewhat less important in high-speed designs
  - This error is a slow change in output voltage, when in hold mode, caused by effects such as leakage currents due to capacitor leakage and reverse-biased junctions.
  - In most CMOS designs using advanced processes, this droop rate is so small and can often be ignored with high S/H frequency.

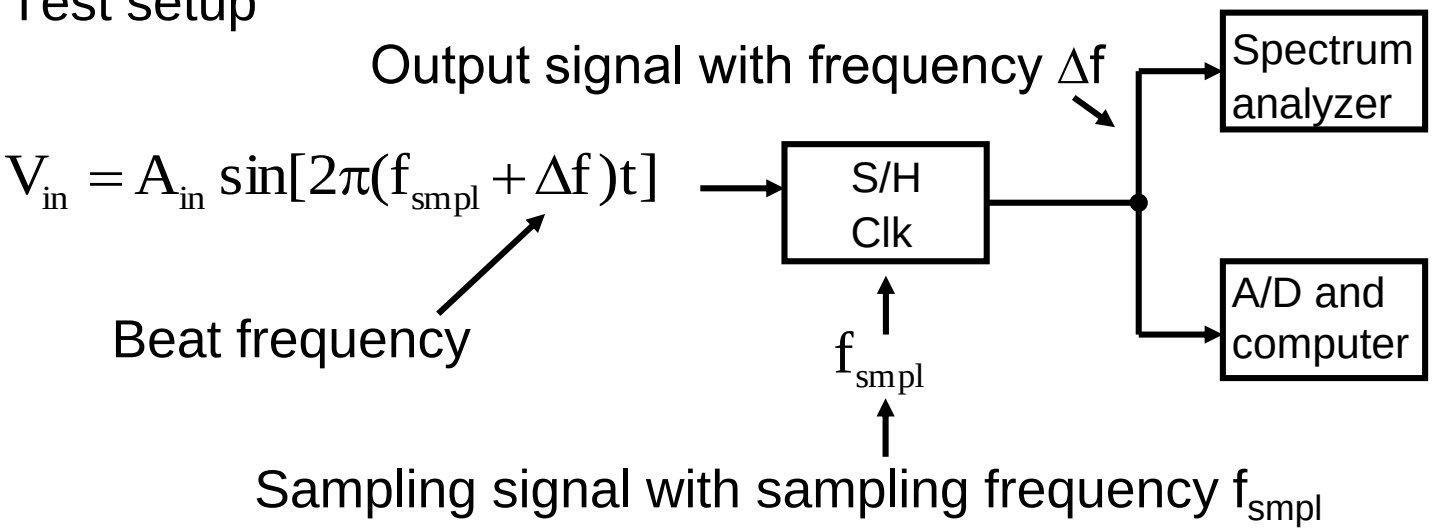
Performance Parameters of S/Hs (Cont.)

- Aperture jitter or aperture uncertainty
  - Result of the effective sampling time changing from one sampling instance to the next
  - More pronounced for high-speed signals. Specifically, when high-speed signals are being sampled, the input signal changes rapidly, resulting in small amounts of aperture uncertainty causing the held voltage to be significantly different from the ideal held voltage.

- Other parameters such as
  - Dynamic range
  - Linearity
  - Gain error
  - Offset error
  - Etc.

Testing S/Hs

- Beat test, a popular method for testing S/Hs
- Test setup

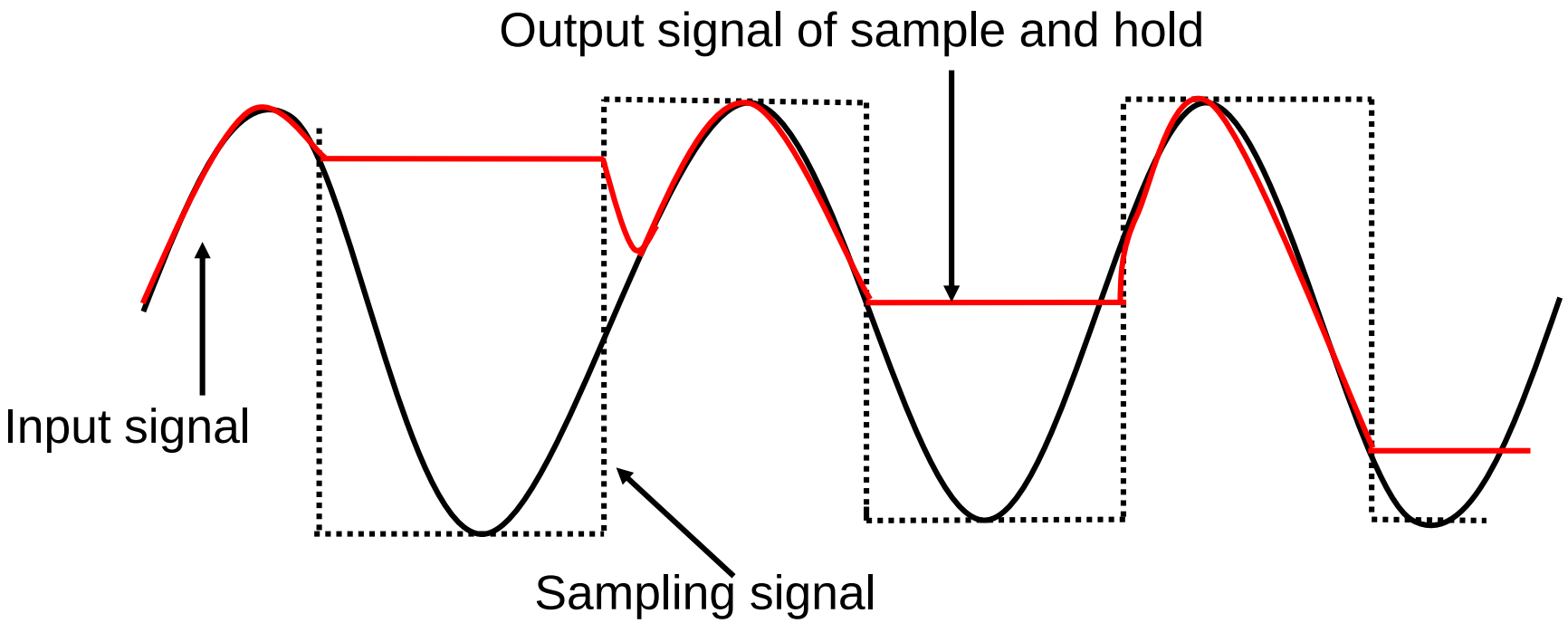


Where the S/H is operating at it's maximum sampling frequency

- Only a relatively low-frequency output signal must be monitored.
- The ideal sinusoidal wave at the beat frequency is subtracted from the measured signal. The error signal is then analyzed for RMS content and spectral components using FFT (Fast Fourier Transform).

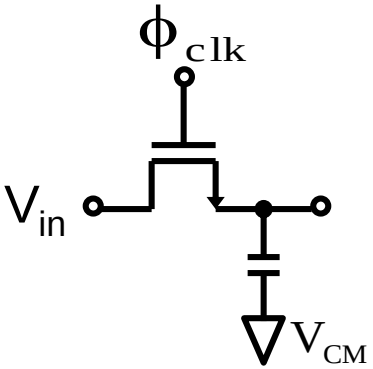
Testing S/Hs (Cont.)

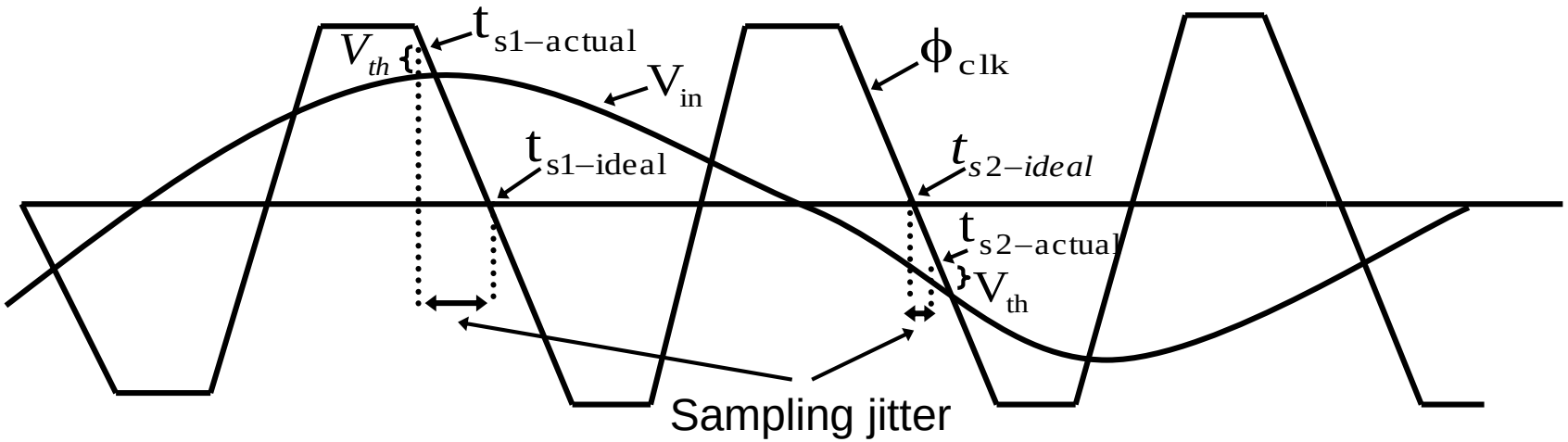
- Example waveforms for the above test setup



MOS S/H Basics

- Two error sources due to switch
  a. Channel charge-injection
  b. Clock feedthrough
  where a is usually larger than b.
- Time jitter
  - Caused by clock waveforms having finite slopes

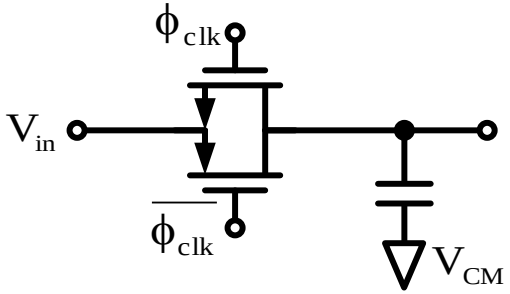




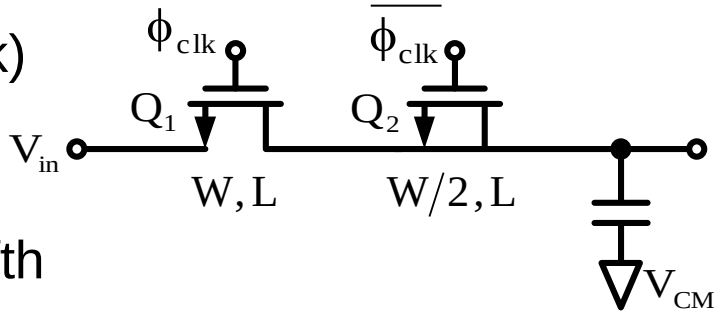
  - When Vin is above 0V, the true sampling time is earlier than the ideal sampling time.
  - When Vin is less than 0V, the true sampling time is late.

Methods for Minimizing Signal-Dependent Switch Error

- Replace n-channel switches by CMOS transmission gates.
  - Transistor turn-off times are signal dependent and this signal dependence causes the n-channel transistor to turn off at different times than the p-channel transistor.
  - PMOS and NMOS have different amount of channel charges, e.g., when V_{in} is closer to V_{DD} , the charge from the p-channel transistor is greater than that from the n-channel transistor



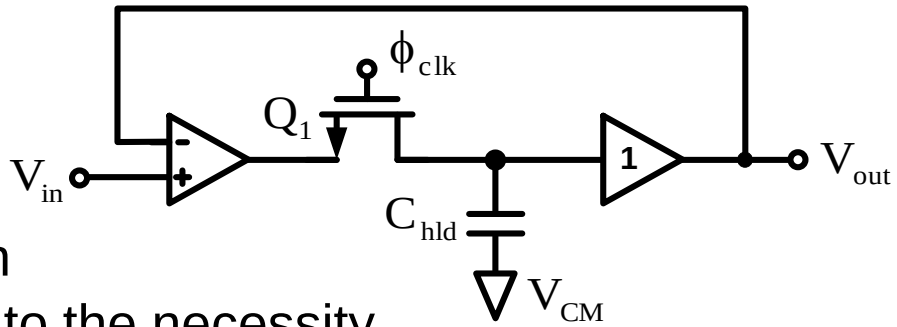
- Add a dummy switch (better with fast clock)
  - When clock waveforms are fast, this technique usually can minimize the hold pedestal to less than about one-fifth the value it would have without it.

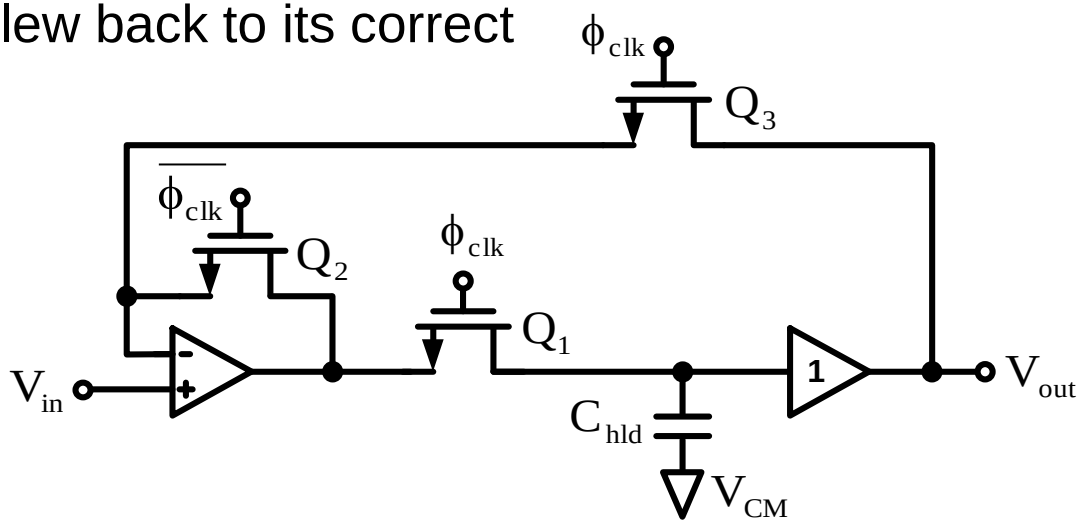


  - The clock of Q_2 changes slightly after that of Q_1. This guarantees that the cancelling charge of Q_2 can't escape through Q_1.

Methods for Minimizing Signal-Dependent Switch Error(Cont.)

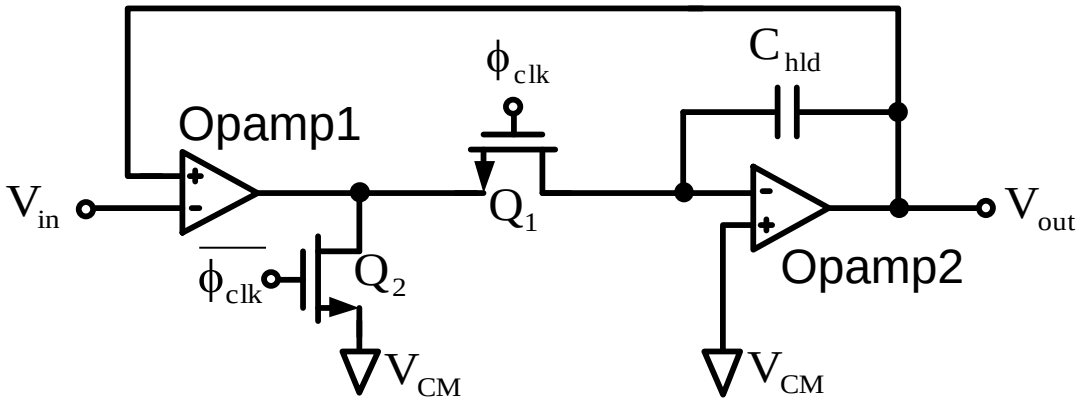
- Include an OPAMP in a feedback loop of a S/H
  - High input impedance
  - The speed of operation can be seriously degraded due to the necessity of guaranteeing that the loop is stable when it is closed.
  - When in hold mode, the OPAMP is open loop, resulting in its output almost certainly saturating at one of the power supply voltages.
  - When the S/H goes back into track mode, it will take some time for the OPAMP output to slew back to its correct closed-loop value. This slewing time can be greatly minimized by adding two additional transistors, Q_2 and Q_3.





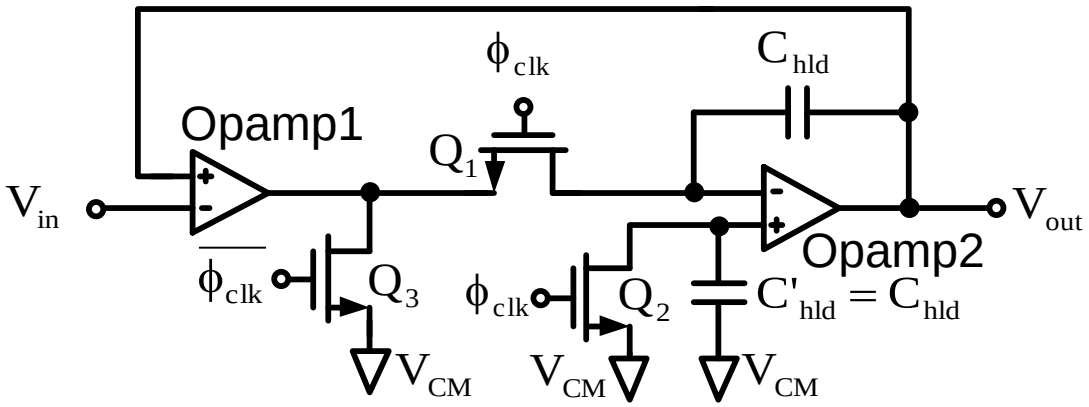
Methods for Minimizing Signal-Dependent Switch Error(Cont.)

- A feedback S/H with a Miller capacitor as a holding capacitor.
  - The voltages on both sides of switch Q_1 are very nearly signal independent.
    - Charge injection results in just a dc offset and will be signal independent.
  - The use of Q_2 greatly speeds up the time it takes the S/H to return to track mode. The use of Q_2 also greatly minimizes signal feedthrough when the S/H is in hold mode.
  - There are two OPAMPs in the loop. $\Rightarrow$ Speed is degraded.



Methods for Minimizing Signal-Dependent Switch Error(Cont.)

- A feedback S/H with clock-feedthrough cancellation circuitry
  - To match charge injection by introducing C_{hld}' (=C_{hld})
  - The major limitation is a second-order effect caused by a mismatch in impedance levels at the left of Q_1 and the bottom of Q_2.



CMOS Multiplier Circuit

- CMOS differential pair can be employed in a multiplier circuit [1][2]

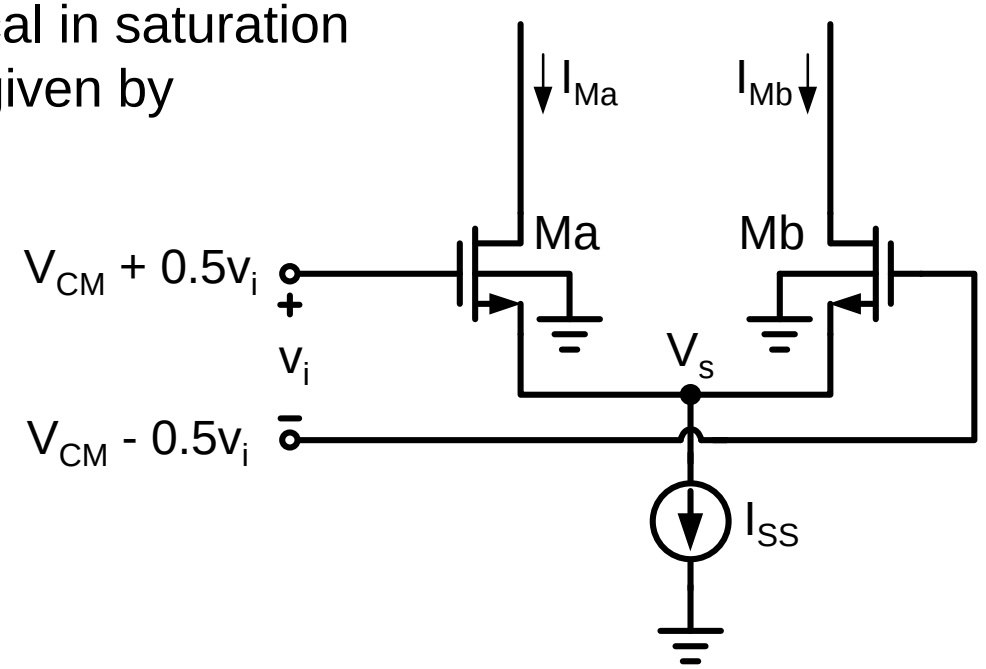
Assume: Ma, Mb are identical in saturation region, the drain current is given by

$$I_D = k(V_{GS} - V_{TH})^2$$

we have

$$\begin{cases} I_{Ma} + I_{Mb} = I_{SS} \\ I_{Ma} = k(V_X + 0.5v_i)^2 \\ I_{Mb} = k(V_X - 0.5v_i)^2 \end{cases}$$

where $V_X = V_{CM} - V_S - V_{TH}$

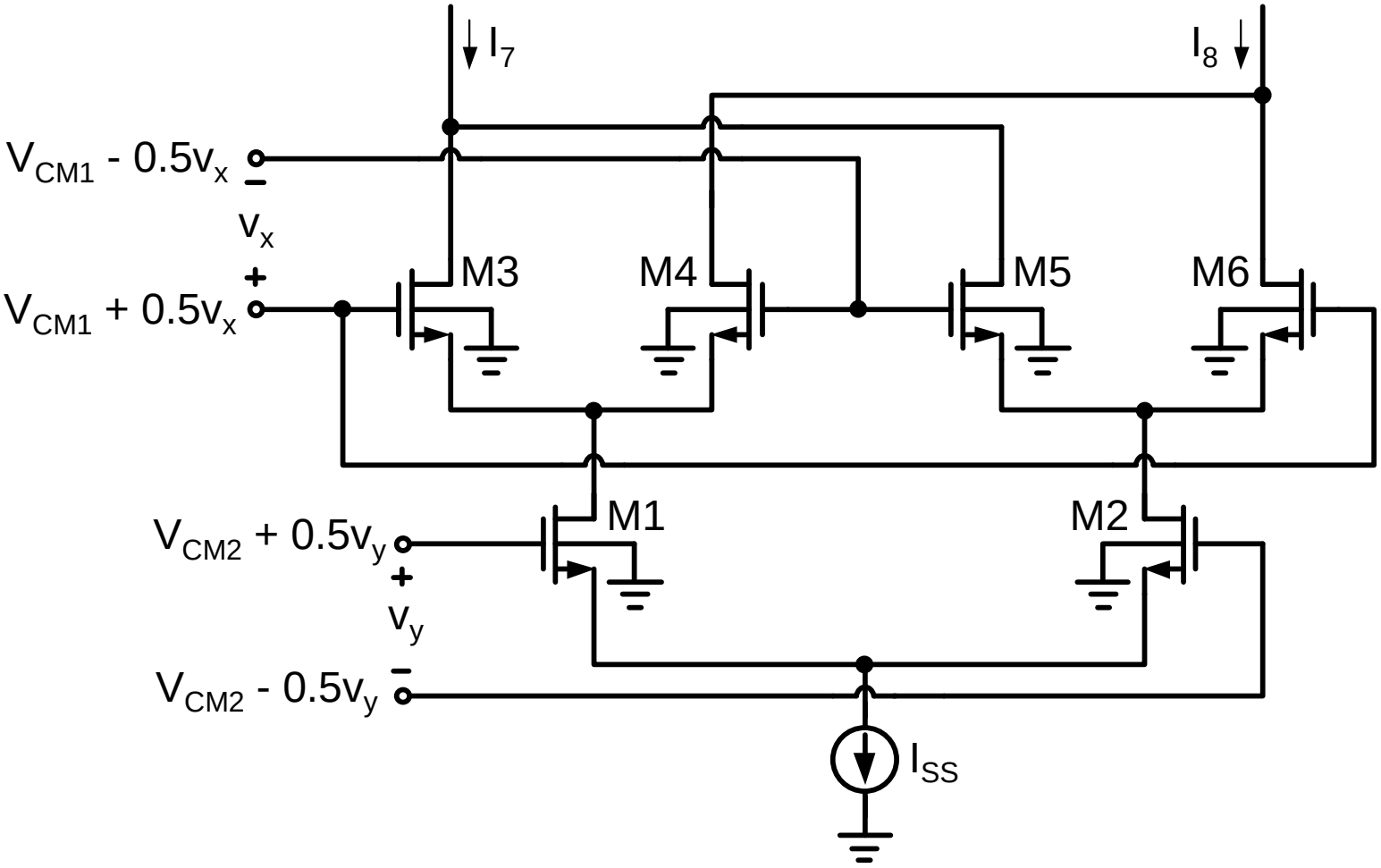


$$\Rightarrow I_{Ma} = \frac{I_{SS}}{2} + \frac{kv_i}{2}\sqrt{\frac{2I_{SS}}{k} - v_i^2} \quad , \quad I_{Mb} = \frac{I_{SS}}{2} - \frac{kv_i}{2}\sqrt{\frac{2I_{SS}}{k} - v_i^2} \qquad \text{------ (1)}$$

$$\Rightarrow \Delta I = I_{Ma} - I_{Mb} = kv_i\sqrt{\frac{2I_{SS}}{k} - v_i^2} \qquad \text{---------- (2)}$$

CMOS Multiplier Circuit (Cont.)

- This MOS version of Gilbert's six-transistor cell is the basic multiplier.
- v_x and v_y can be made positive or negative: Four-quadrant multiplier



CMOS Multiplier Circuit (Cont.)

- Define: input signal v_x and v_y , the output current $I_{out} = I_7 - I_8$

$$\Rightarrow I_{out} = I_7 - I_8 = (I_{M3} + I_{M5}) - (I_{M4} + I_{M6}) = (I_{M3} - I_{M4}) - (I_{M6} - I_{M5})$$

- Refer to 8-12, equation (1)

$$\Rightarrow I_{M1} = \frac{I_{SS}}{2} + \frac{kv_y}{2}\sqrt{\frac{2I_{SS}}{k} - v_y^2}\ , \quad I_{M2} = \frac{I_{SS}}{2} - \frac{kv_y}{2}\sqrt{\frac{2I_{SS}}{k} - v_y^2}$$

- Refer to 8-12, equation (2) and assuming v_x is sufficient small

$$\Rightarrow I_{M3} - I_{M4} = kv_x\sqrt{\frac{I_{SS}}{k} + v_y\sqrt{\frac{2I_{SS}}{k} - v_y^2} - v_x^2} = kv_x\sqrt{\left(\sqrt{\frac{I_{SS}}{k} - \frac{v_y^{\ 2}}{2}} + \frac{v_y}{\sqrt{2}}\right)^2}$$

$$\Rightarrow I_{M6} - I_{M5} = kv_x\sqrt{\frac{I_{SS}}{k} - v_y\sqrt{\frac{2I_{SS}}{k} - v_y^2} - v_x^2} = kv_x\sqrt{\left(\sqrt{\frac{I_{SS}}{k} - \frac{v_y^{\ 2}}{2}} - \frac{v_y}{\sqrt{2}}\right)^2}$$

$$\Rightarrow I_{out} = (I_{M3} - I_{M4}) - (I_{M6} - I_{M5}) = \sqrt{2}kv_x v_y$$

References:

[1]J. N. Babanezhad and G. C. Temes, “A 20-V four-quadrant CMOS analog multiplier”, *IEEE J. Solid-State Circuits*, vol. SC-20, pp.1158-1168, Dec. 1985.

[2]Gunhee Han and Edgar Sanchez-Sinencio, “CMOS Transconductance Multipliers: A Tutorial”, *IEEE Trans. Circuit Syst. II*, vol. 45, pp.1550-1563, Dec. 1998.

Voltage and Current References

- Circuits that yield a precise DC voltage or current independent of external influences are called voltage references(V_{ref}) or current references (I_{ref})

- Two major specs on V_{ref} and I_{ref}
  - Temperature Coefficient
  - Power Supply Sensitivity

Power Supply Sensitivity of V_{ref}/I_{ref}

- The sensitivity of V_{ref} to change in a power supply V_{xx} (V_{DD} or GND) is given as:

$$S_{V_{XX}}^{V_{REF}} = \lim_{\Delta V_{XX} \to 0} \frac{\Delta V_{REF} / V_{REF}}{\Delta V_{XX} / V_{XX}}$$

$$= \frac{V_{XX}}{V_{REF}} \left(\frac{\partial V_{REF}}{\partial V_{XX}} \right)$$

- Once $S_{V_{XX}}^{V_{REF}}$ is known, we obtain

$$\frac{\Delta V_{REF}}{V_{REF}} \approx S_{V_{XX}}^{V_{REF}} \left(\frac{\Delta V_{XX}}{V_{XX}} \right)$$

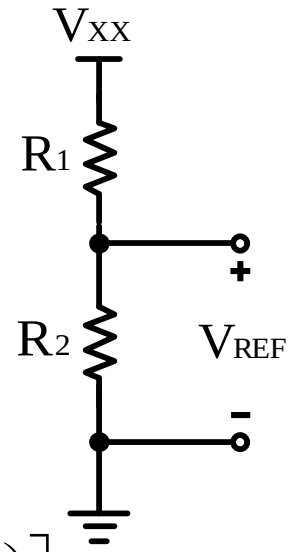
- Besides,
  $S_{V_{XX}}^{I_{REF}}$ and $\frac{\Delta I_{REF}}{\Delta V_{XX}}$ can be similarly obtained

Temperature Coefficient of V_{REF}/I_{REF}

- $TC(V_{REF}) = \frac{1}{V_{REF}} \frac{\partial V_{REF}}{\partial T} = \frac{1}{T} S_T^{V_{REF}}$; $TC(I_{REF}) = \frac{1}{I_{REF}} \frac{\partial I_{REF}}{\partial T} = \frac{1}{T} S_T^{I_{REF}}$

- Examples(resistor divider):
  - Voltage Sensitivity

$$V_{REF} = V_{XX}\left(\frac{R_2}{R_1+R_2}\right) \Rightarrow S_{V_{XX}}^{V_{REF}} = \frac{V_{XX}}{V_{REF}} \frac{\partial V_{REF}}{\partial V_{XX}} = 1$$



  - Temperature Coefficient

$$TC(V_{REF}) = \frac{1}{V_{REF}} \frac{\partial V_{REF}}{\partial T} = \frac{Vxx}{V_{REF}} \left[\frac{\partial}{\partial T}\left(\frac{R_2}{R_1+R_2}\right)\right]$$

$$= \frac{Vxx}{V_{REF}} \left[\frac{1}{R_1+R_2}\frac{\partial R_2}{\partial T} + R_2 \frac{-1}{(R_1+R_2)^2}\left(\frac{\partial R_1}{\partial T} + \frac{\partial R_2}{\partial T}\right)\right]$$

$$= \frac{V_{XX}}{V_{REF}} \frac{R_1 R_2}{(R_1+R_2)^2}\left(\frac{1}{R_2}\frac{\partial R_2}{\partial T} - \frac{1}{R_1}\frac{\partial R_1}{\partial T}\right)$$

If $TC(R_1)=TC(R_2)$, then $TC(V_{REF})=0$

Supply Independent Current Source

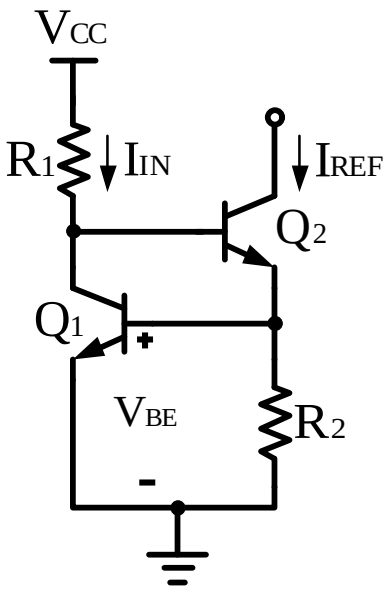
- Neglecting base current

$$I_{REF} = V_{BE1}/R_2 = \left(V_t/R_2\right)\ln\left(I_{IN}/I_{S1}\right)$$

$$I_{IN} \approx \left(V_{CC} - 2V_{BE}\right)/R_1$$

$$S_{V_{CC}}^{I_{REF}} = \frac{V_{CC}}{I_{REF}}\frac{\partial I_{REF}}{\partial V_{CC}}$$

$$\approx \frac{V_{CC}}{I_{REF}}\frac{V_t}{R_2}\frac{R_1 I_{S1}}{V_{CC} - 2V_{BE}}\frac{1}{R_1 I_{S1}}$$



- Assuming $V_{CC} >> 2V_{BE}$

$$\Rightarrow S_{V_{CC}}^{I_{REF}} \approx \frac{V_t}{I_{REF}R_2}$$

Reducing TC(V_{REF}) by using the combination of Breakdown diode and pn diode

- Breakdown diodes and pn junction diodes(or transistor connected diodes) have opposite temperature coefficients.

$$V_{REF} = \frac{R_2}{R_1 + R_2}(V_Z - 3V_{BE}) + V_{BE}$$

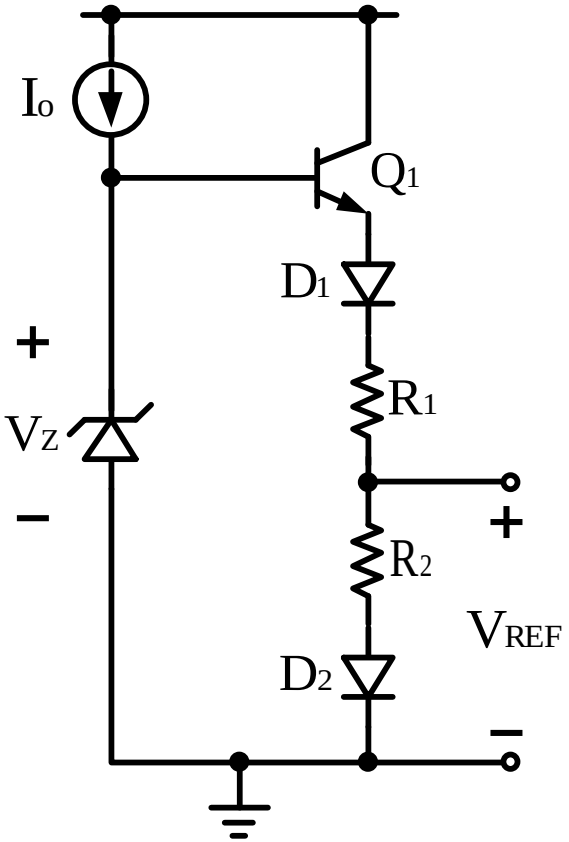
$$= \left(\frac{R_2}{R_1 + R_2}\right)V_Z - 2\left(\frac{R_2}{R_1 + R_2}\right)V_{BE} + \frac{R_1}{R_1 + R_2}V_{BE}$$

- Let $\frac{\partial V_{REF}}{\partial T} = 0$, then

$$\frac{\frac{\partial V_Z}{\partial T}}{\frac{\partial V_{BE}}{\partial T}} = 2 - \frac{R_1}{R_2}$$

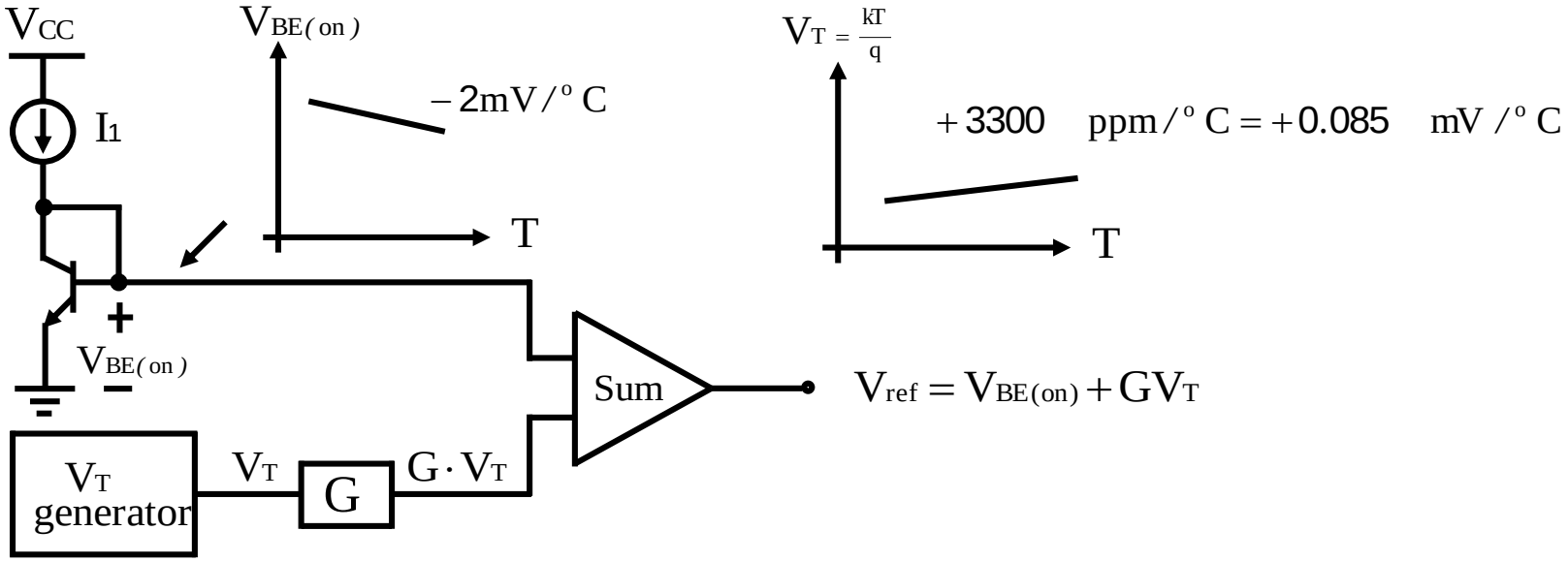
Assuming $\frac{\partial V_Z}{\partial T} \approx 3mV^oC^{-1}$ and $\frac{\partial V_{BE}}{\partial T} \approx -2mV^oC^{-1}$

then $\frac{R_1}{R_2} = 3.5$ and $V_{REF} \approx 1.4V$



Bandgap Voltage Reference

- Model



- Rough calculation
  V_{BE} has a temperature coefficient of –2 mV/°C at room temperature
  V_T has a temperature coefficient of 0.085 mV/°C
  $V_{REF}=V_{BE}+GV_T$

- Assuming V_{BE}=0.65V, then G=23.5 & V_{REF}=1.26V =>TC=0

Bandgap Voltage Reference (Cont.)

- The most popular approach to realize voltage reference for CMOS and bipolar ICs
- Cancelling the negative temperature dependence of a pn junction with a positive temperature dependence from a PTAT(proportional-to-absolute-temperature) circuit
- Accurate calculation

  A forward-biased base-emitter junction of a bipolar transistor has an I-V relationship given by $I_C = I_S e^{qV_{BE}/kT}$

  where I_s is the transistor scale (reverse saturation) current and, although not shown, has a strong dependence on temperature.

  Writing the base-emitter voltage as a function of collector current and temperature, it can be shown that [Brugler, 1967; Tsividis, 1980]

$$V_{BE}(T) = V_{G0}\left(1-\frac{T}{T_0}\right) + V_{BE0}\frac{T}{T_0} + \frac{mkT}{q}\ln\left(\frac{T_0}{T}\right) + \frac{kT}{q}\ln\left(\frac{J_C}{J_{C0}}\right)$$

Bandgap Voltage Reference(Cont.)

Here, V_{G0} is the bandgap voltage of silicon extrapolated to 0^{o}k (approximately 1.206V), k is Boltzmann's constant, and m is a temperature constant approximately equal to 2.3. Also, J_C and T are the collector current density and temperature, respectively, while the subscript 0 designates an appropriate quantity at a reference temperature, T_0 .

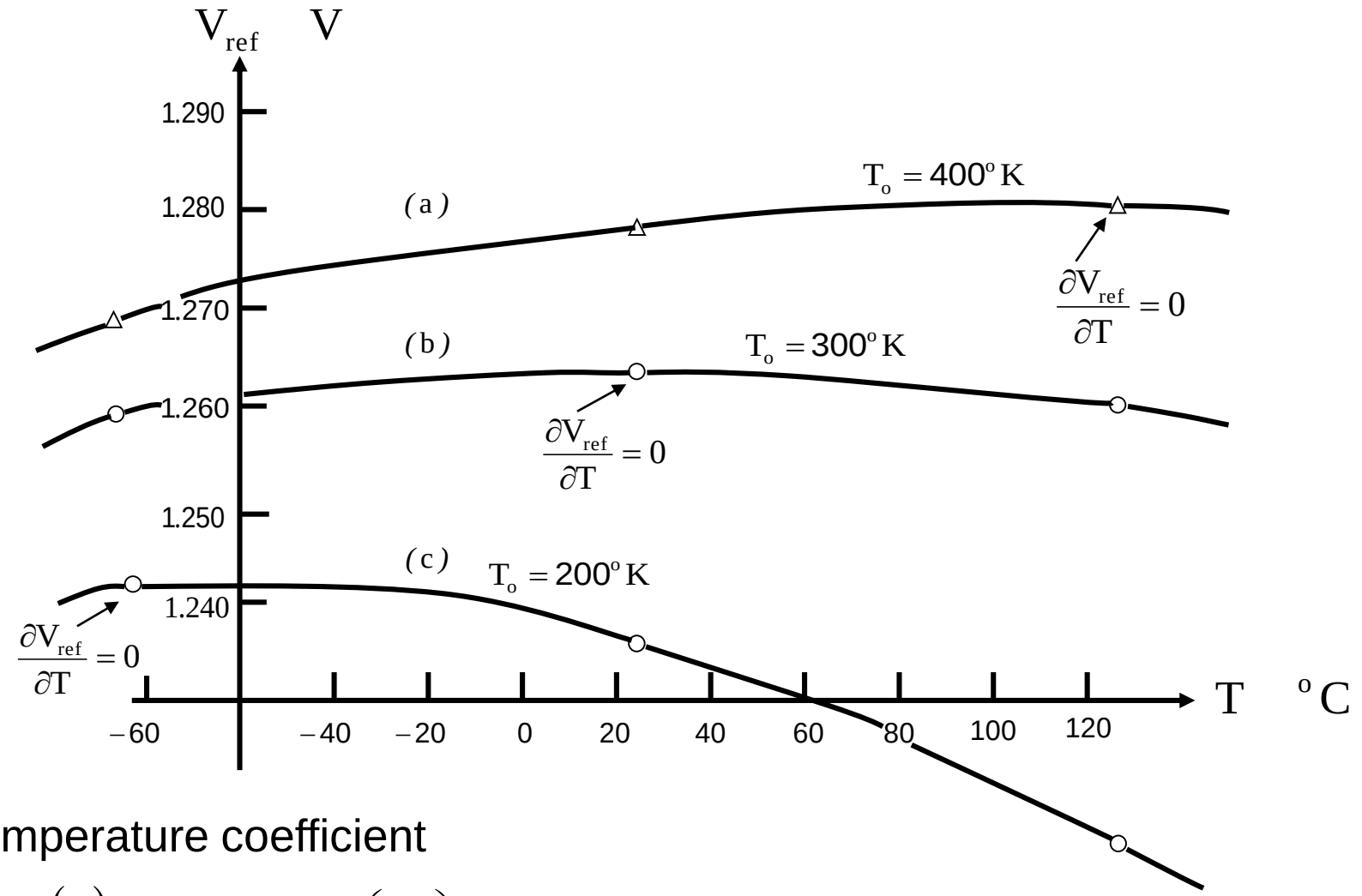
Specifically, J_{C0} is the collector current density at the reference temperature, T_0, whereas J_C is the collector current density at the true temperature, T. Also, V_{BE0} is the junction voltage at the reference temperature, T_0, whereas V_{BE} is the base-emitter junction voltage at the true temperature, T.

$$V_{ref}(T) = V_{BE}(T) + GV_T$$

$$= V_{G0} + (m-1)\frac{kT}{q}\left(1 + \ln\frac{T_0}{T}\right)$$

↑ if G is properly taken

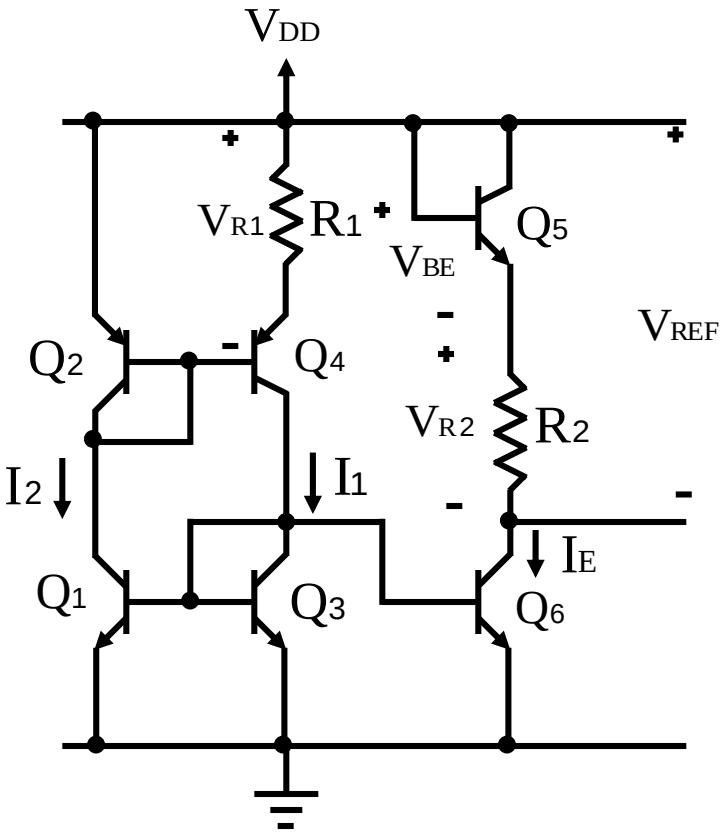
Bandgap Voltage Reference(Cont.)



- Temperature coefficient

$$\frac{\partial V_{ref}(T)}{\partial T} = (m-1)\frac{k}{q}\cdot \ln\left(\frac{T_0}{T}\right)$$

Bipolar Bandgap Voltage Reference



$$\frac{I_2}{I_1}=\frac{I_{S1}}{I_{S3}} \quad \text{——} \ ①$$

$$I_1=I_{S4}e^{V_{BE4}/V_t} \text{ and } I_2=I_{S2}e^{V_{BE2}/V_t}$$

$$-V_{BE2} = -V_{BE4} + V_{R1}$$

From ①

$$\frac{I_2}{I_1}=\frac{I_{S1}}{I_{S3}}=\frac{I_{S2}\exp\left(\frac{-V_{BE4}+V_{R1}}{V_t}\right)}{I_{S4}\exp\left(\frac{-V_{BE4}}{V_t}\right)}=\frac{I_{S2}}{I_{S4}}\exp\left(\frac{V_{R1}}{V_t}\right)$$

$$\Rightarrow V_{R1}=V_t \ln\frac{I_{S1}I_{S4}}{I_{S2}I_{S3}}$$

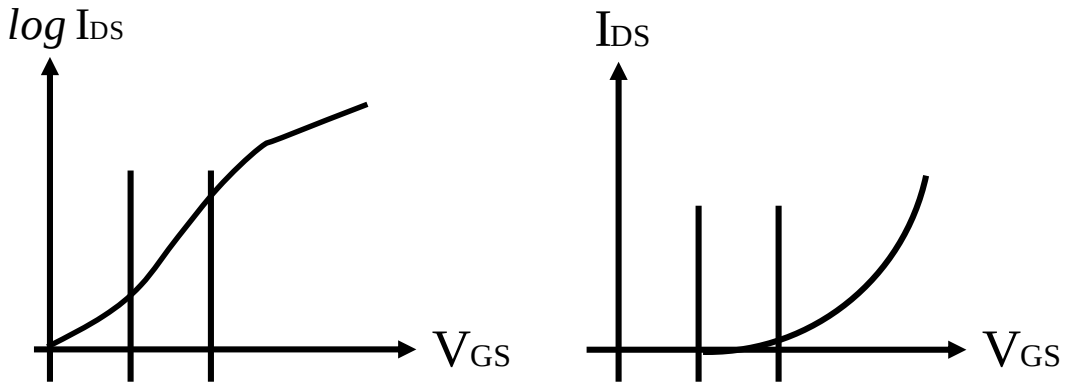
$$V_{REF}=V_{BE}+I_E R_2=V_{BE}+I_1\frac{I_{S6}}{I_{S3}}R_2=V_{BE}+\frac{V_{R1}}{R_1}\frac{I_{S6}}{I_{S3}}R_2$$

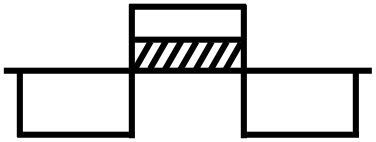
$$=V_{BE}+\left(\frac{R_2}{R_1}\right)\left(\frac{I_{S6}}{I_{S3}}\right)V_t\times\ln\left(\frac{I_{S1}I_{S4}}{I_{S2}I_{S3}}\right)$$

- Operational principle:
  - Initial loop gain > 1
  - Equilibrium is achieved when loop gain is reduced to 1 by V_{R1} across R

CMOS Bandgap Voltage Reference in Weak Inversion

- Weak inversion (I-V is similar to bipolar)





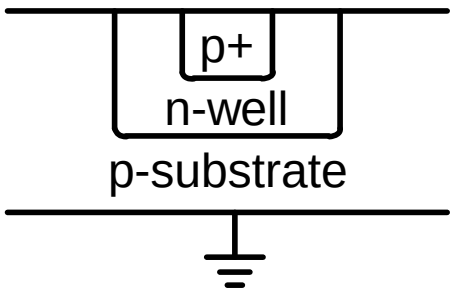
near off : weak inversion

on : strong inversion

$$I_{DS} = \frac{W}{L} I_{D0} \exp^{-V_{BS}\left[\left(\frac{1}{nV_t}\right)-\left(\frac{1}{V_t}\right)\right]} \left(1-\exp^{-\frac{V_{DS}}{V_t}}\right) \exp^{\frac{V_{GS}-V_{Th}}{nV_t}}$$

$$\text{where } V_t = \frac{kT}{q} \text{ and } V_{Th} \text{ is threshold voltage}$$

- Parasitic bipolar transistor is needed.
  (Example with N-well process)



CMOS Bandgap Voltage Reference in Weak Inversion (Cont.)

- A CMOS bandgap voltage reference operating in weak inversion

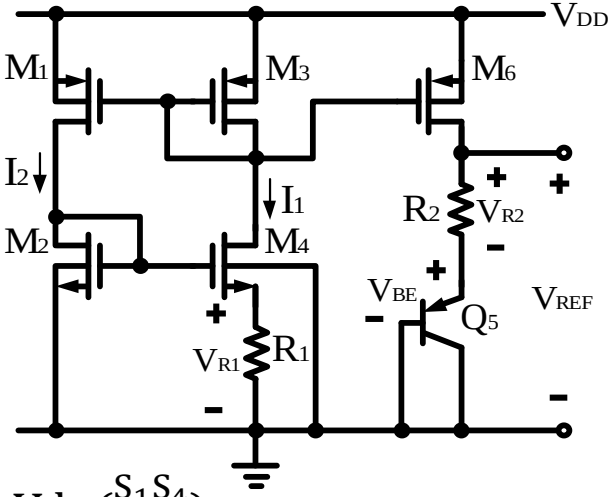
$$I_{DS} = \frac{W}{L} I_{D0} \exp(V_{eff}/nV_t)(1 - \exp(-V_{DS}/nV_t))$$

$$\text{If } V_{DS} \gg V_t \Rightarrow I_{DS} \approx \left(\frac{W}{L}\right) I_{D0} \exp\left(-\frac{V_{BS}}{nV_t} + \frac{V_{BS}}{V_t} + \frac{V_{GS}-V_{Th}}{nV_t}\right) = \left(\frac{W}{L}\right) I_{D0} \exp\left(\frac{V_{GB}-V_{Th}}{nV_t} + \frac{V_{BS}}{V_t}\right)$$

$$\frac{I_2}{I_1} = \frac{(W/L)_{M1}}{(W/L)_{M3}} \Rightarrow I_2 \approx \left(\frac{W}{L}\right)_{M2} I_{D0} \exp\left(\frac{V_{GB2}-V_{Th}}{nV_t} + \frac{V_{BS2}}{V_t}\right)$$

$$I_1 \approx \left(\frac{W}{L}\right)_{M4} I_{D0} \exp\left(\frac{V_{GB4}-V_{Th}}{nV_t} + \frac{V_{BS4}}{V_t}\right)$$

If channel length modulation effect is ignored $\Rightarrow V_{BS2} \neq V_{BS4}, V_{BS2} = 0, V_{BS4} = -V_{R1}$



$$\text{Let } \left(\frac{W}{L}\right) = S$$

$$\Rightarrow \frac{I_2}{I_1} = \frac{S_1}{S_3} = \frac{S_2 I_{D0} \exp\left(\frac{V_{GB2}-V_{Th}}{nV_t} + \frac{V_{BS2}}{V_t}\right)}{S_4 I_{D0} \exp\left(\frac{V_{GB4}-V_{Th}}{nV_t} + \frac{V_{BS4}}{V_t}\right)} \Rightarrow V_{R1} = -V_{BS4} = V_t \ln\left(\frac{S_1 S_4}{S_2 S_3}\right)$$

$$\Rightarrow V_{REF} = V_{BE} + \left(\frac{R_2}{R_1}\right)\left(\frac{S_6}{S_3}\right) V_t \ln\left(\frac{S_1 S_4}{S_2 S_3}\right)$$

- Precautions:
  - M_2 and M_4 must be in weak inversion
  - Leakage currents must be minimized
  - Large output resistance of the devices for good current mirrors. Using long channel or various mirrors presented before.